FIG.1A

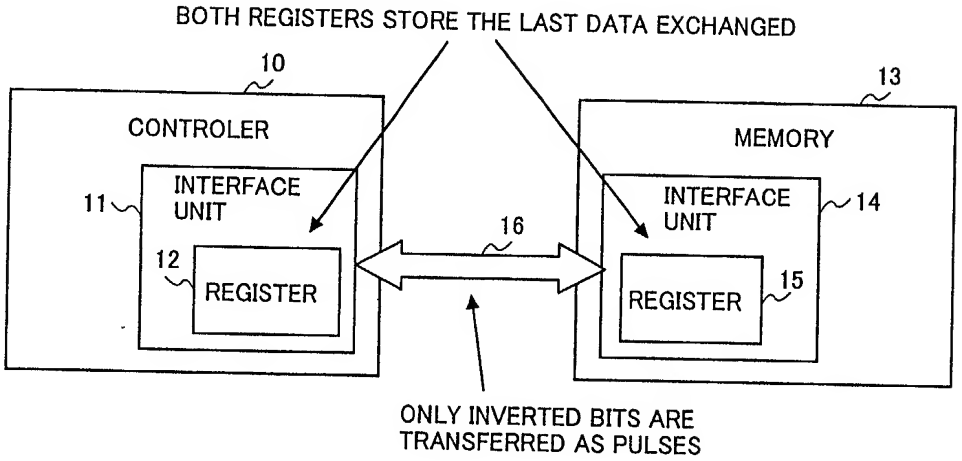

BOTH REGISTERS STORE THE LAST DATA EXCHANGED
10
CONTROLER
11
INTERFACE UNIT
12
REGISTER
16
13
MEMORY
INTERFACE UNIT
14
REGISTER
15
ONLY INVERTED BITS ARE TRANSFERRED AS PULSES

FIG.1B

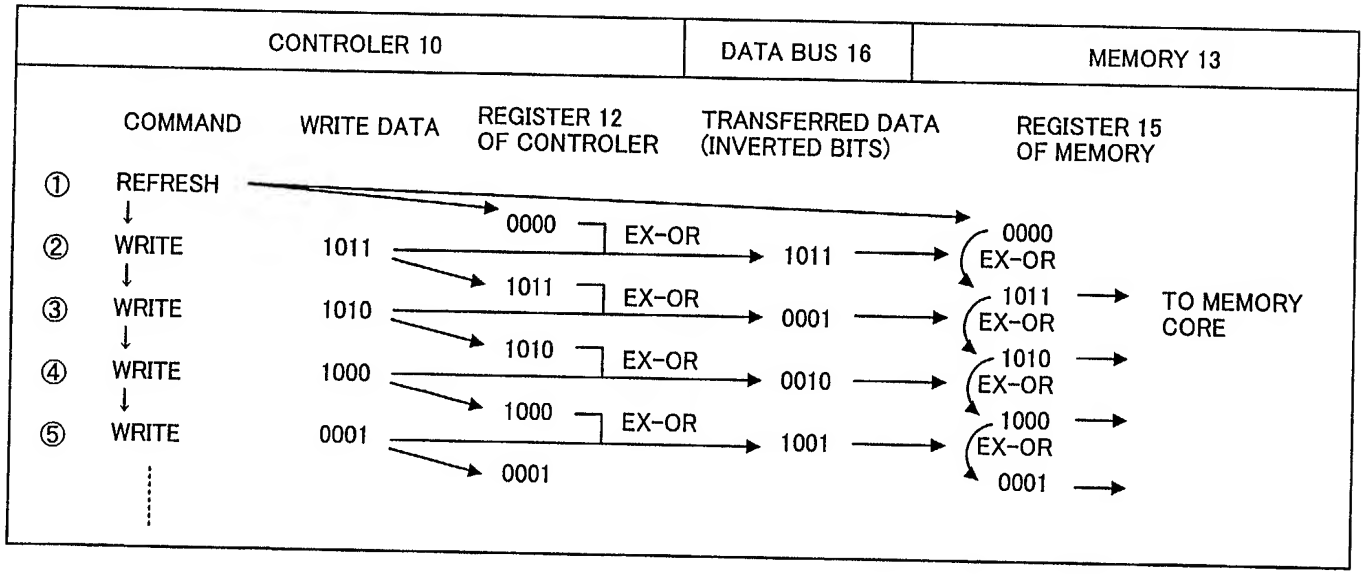

CONTROLER 10
DATA BUS 16
MEMORY 13
COMMAND
WRITE DATA
REGISTER 12 OF CONTROLER
TRANSFERRED DATA (INVERTED BITS)
REGISTER 15 OF MEMORY
① REFRESH
② WRITE
③ WRITE
④ WRITE
⑤ WRITE
1011
1010
1000
0001
0000
EX-OR
TO MEMORY CORE

FIG.2

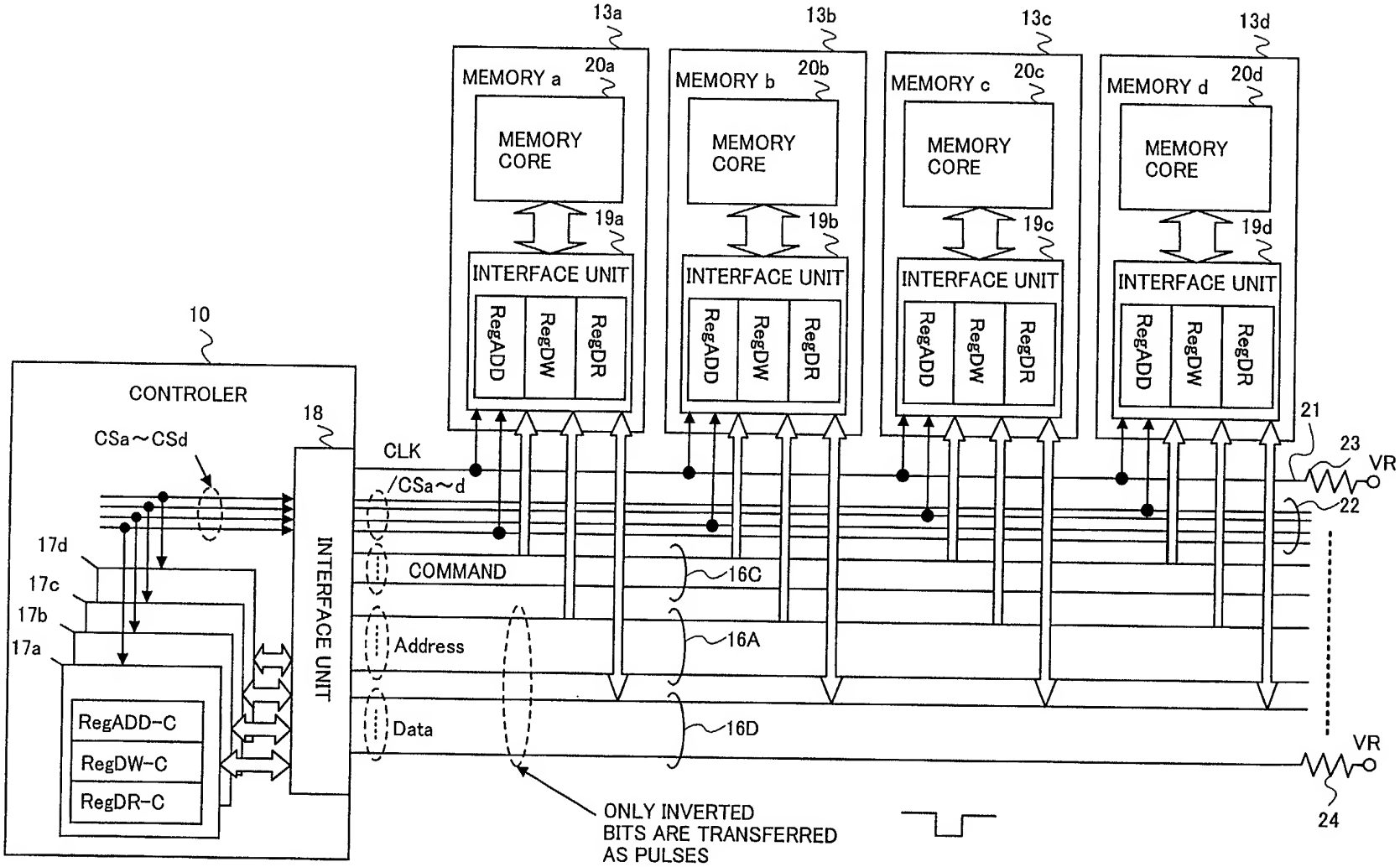

13a
13b
13c
13d
MEMORY a
20a
MEMORY b
20b
MEMORY c
20c
MEMORY d
20d
MEMORY CORE
19a
19b
19c
19d
INTERFACE UNIT
RegADD
RegDW
RegDR
10
CONTROLER
18
CSa~CSd
CLK
/CSa~d
COMMAND
Address
Data
17d
17c
17b
17a
INTERFACE UNIT
RegADD-C
RegDW-C
RegDR-C
16C
16A
16D
21
23
VR
22
VR
24
ONLY INVERTED
BITS ARE TRANSFERRED
AS PULSES

FIG.3

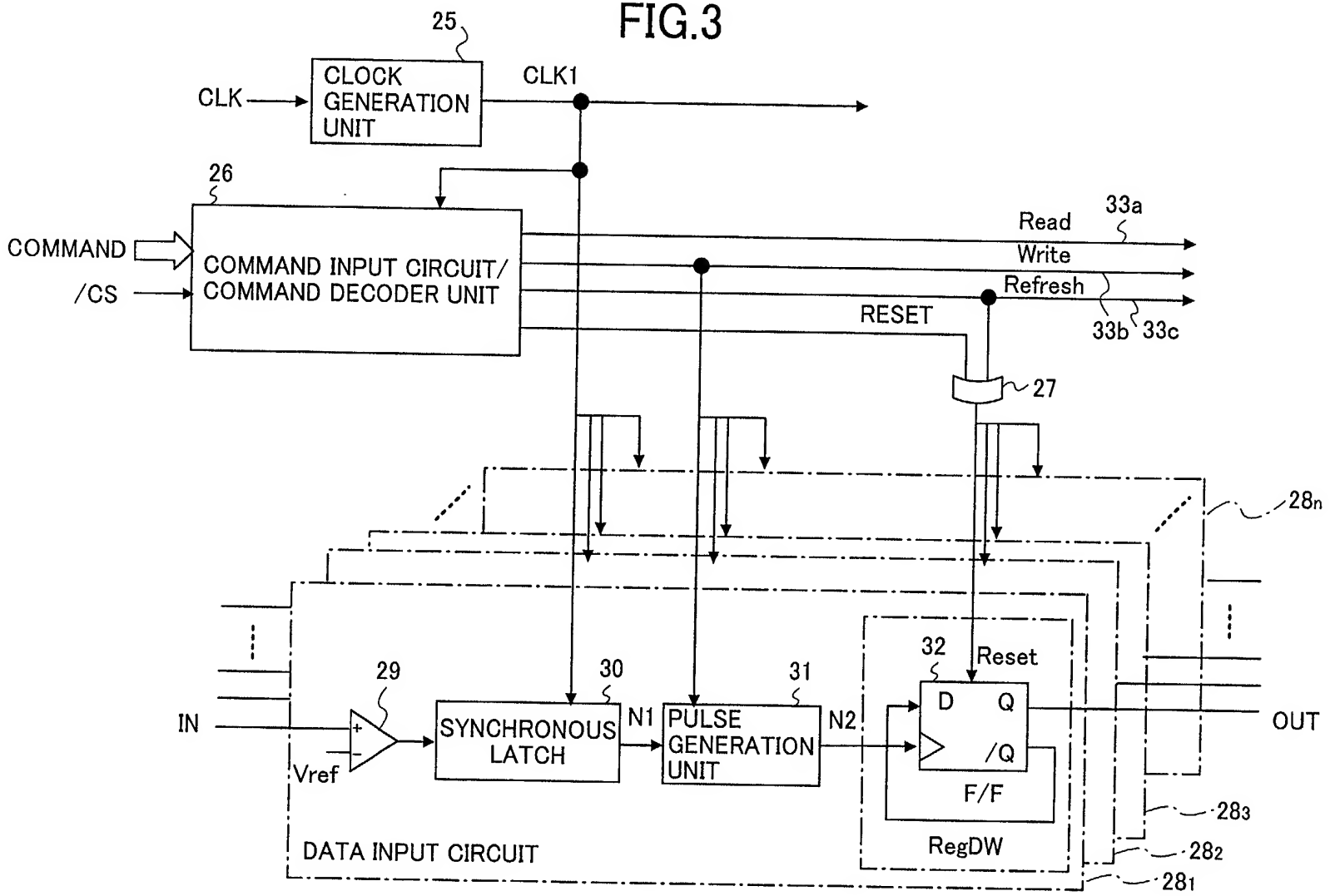

25
CLOCK GENERATION UNIT
CLK
CLK1
26
COMMAND
/CS
COMMAND INPUT CIRCUIT/ COMMAND DECODER UNIT
Read
Write
Refresh
RESET
33a
33b
33c
27
28n
29
30
31
32
Reset
IN
Vref
SYNCHRONOUS LATCH
N1
PULSE GENERATION UNIT
N2
D
Q
/Q
F/F
OUT
DATA INPUT CIRCUIT
RegDW
283
282
281

FIG. 4

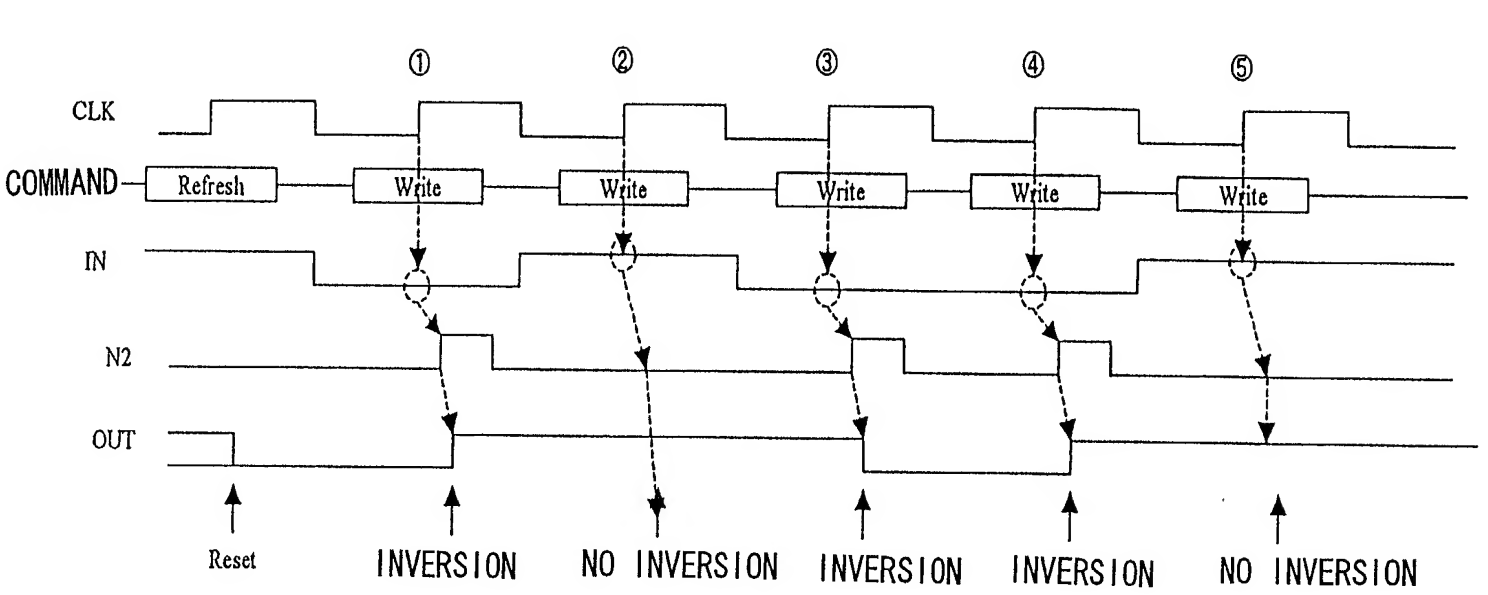

①
②
③
④
⑤
CLK
COMMAND
Refresh
Write
Write
Write
Write
Write
IN
N2
OUT
Reset
INVERSION
NO INVERSION
INVERSION
INVERSION
NO INVERSION

FIG.5

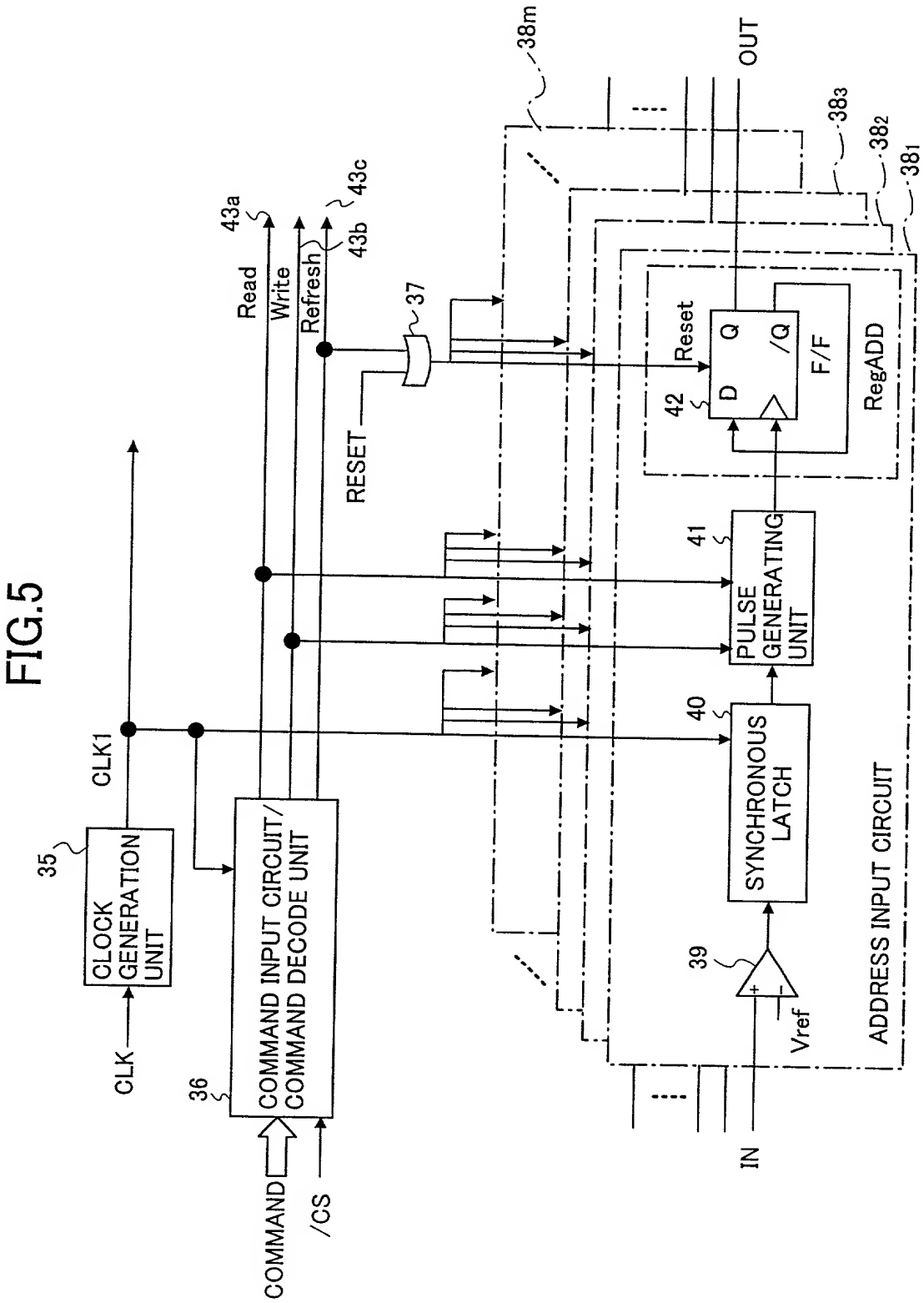

CLOCK GENERATION UNIT
35
CLK
CLK1
COMMAND INPUT CIRCUIT/ COMMAND DECODE UNIT
36
COMMAND
/CS
Read
Write
Refresh
43a
43b
43c
RESET
37
38m
OUT
38₃
38₂
38₁
Reset
D
Q
/Q
F/F
42
RegADD
PULSE GENERATING UNIT
41
SYNCHRONOUS LATCH
40
39
Vref
IN
ADDRESS INPUT CIRCUIT

FIG.6

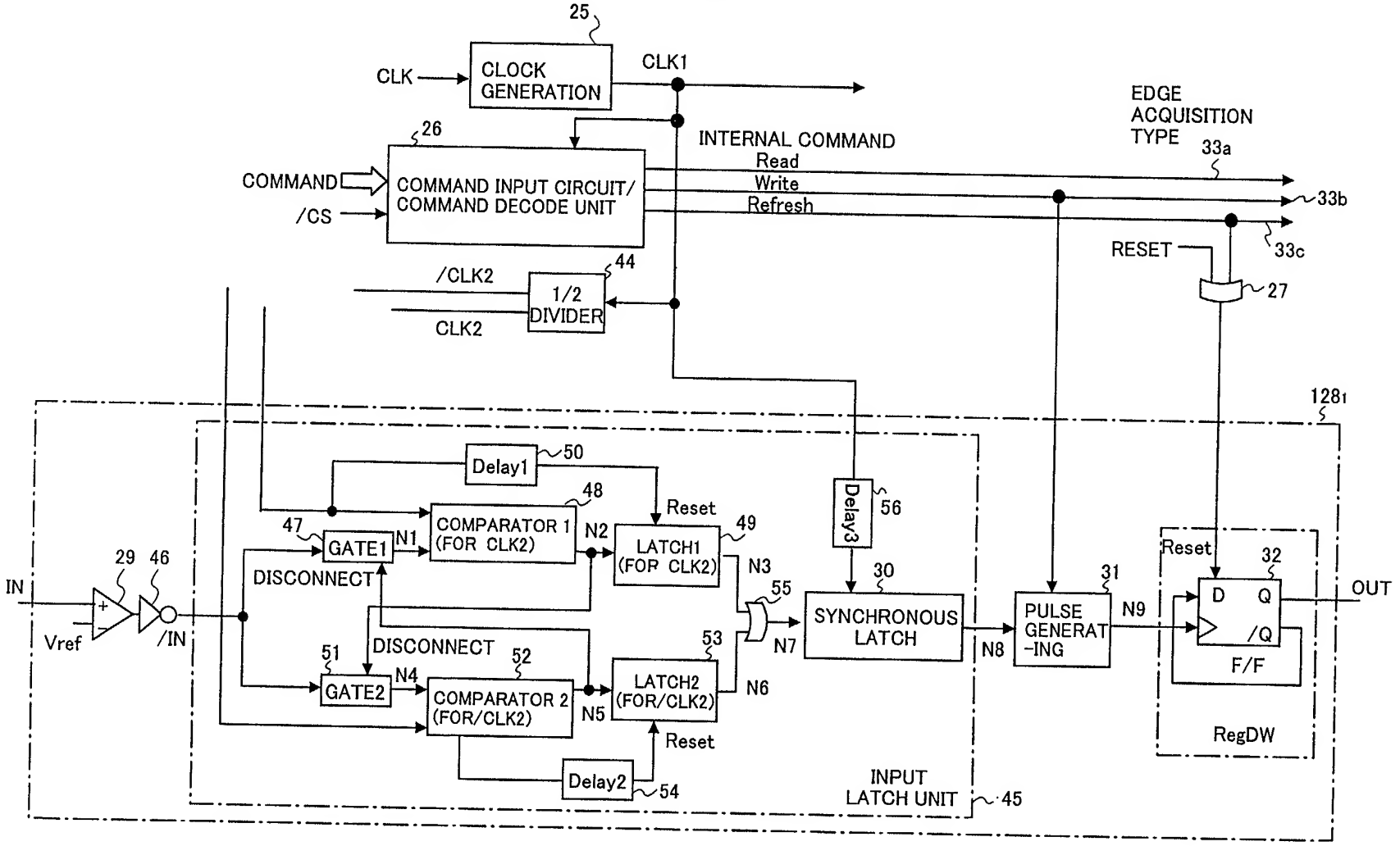

25
CLK
CLOCK GENERATION
CLK1
26
COMMAND
/CS
COMMAND INPUT CIRCUIT/ COMMAND DECODE UNIT
INTERNAL COMMAND
Read
Write
Refresh
EDGE ACQUISITION TYPE
33a
33b
33c
RESET
27
/CLK2
CLK2
1/2 DIVIDER
44
128i
Delay1
50
48
Reset
47
GATE1
N1
COMPARATOR 1 (FOR CLK2)
N2
LATCH1 (FOR CLK2)
49
N3
Delay3
56
30
IN
29
46
Vref
/IN
DISCONNECT
55
SYNCHRONOUS LATCH
N7
N8
31
PULSE GENERAT -ING
N9
Reset
32
D
Q
/Q
F/F
OUT
RegDW
DISCONNECT
51
GATE2
N4
52
COMPARATOR 2 (FOR/CLK2)
N5
LATCH2 (FOR/CLK2)
53
N6
Reset
Delay2
54
INPUT LATCH UNIT
45

FIG.7

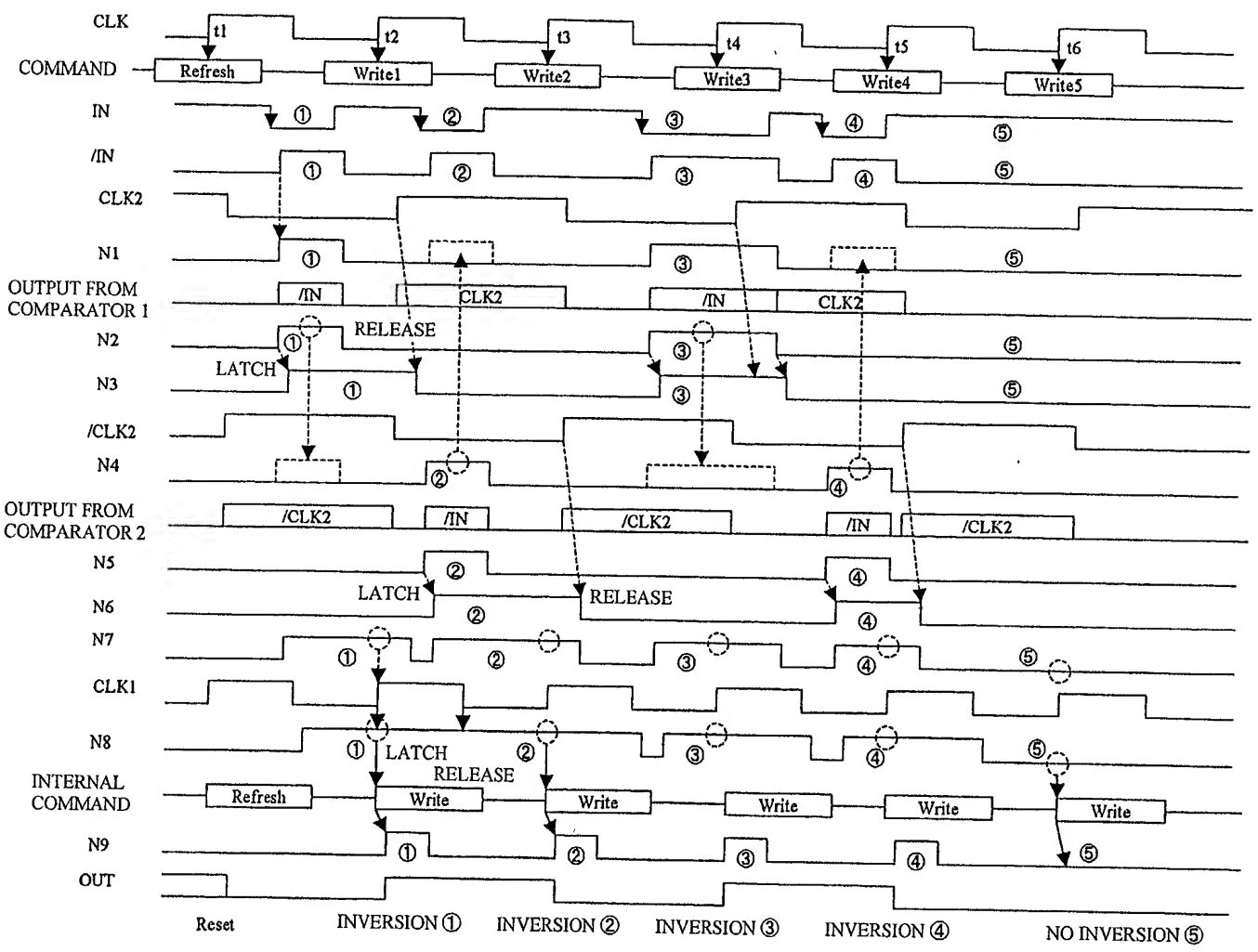

CLK
COMMAND
IN
/IN
CLK2
N1
OUTPUT FROM COMPARATOR 1
N2
N3
/CLK2
N4
OUTPUT FROM COMPARATOR 2
N5
N6
N7
CLK1
N8
INTERNAL COMMAND
N9
OUT
t1
t2
t3
t4
t5
t6
Refresh
Write1
Write2
Write3
Write4
Write5
/IN
CLK2
RELEASE
LATCH
/CLK2
/IN
LATCH
RELEASE
LATCH
RELEASE
Refresh
Write
Write
Write
Write
Write
Reset
INVERSION ①
INVERSION ②
INVERSION ③
INVERSION ④
NO INVERSION ⑤

FIG.8

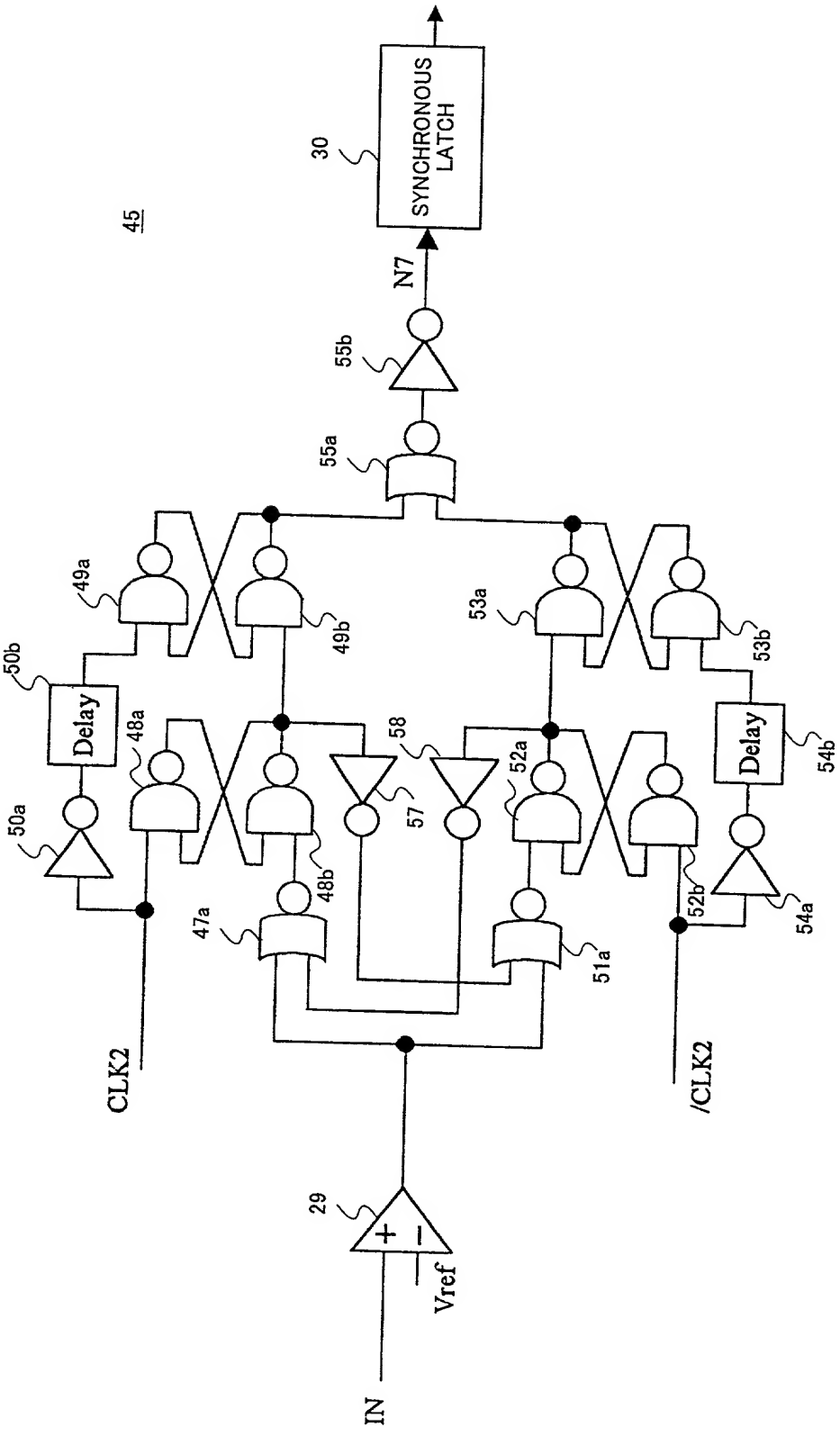
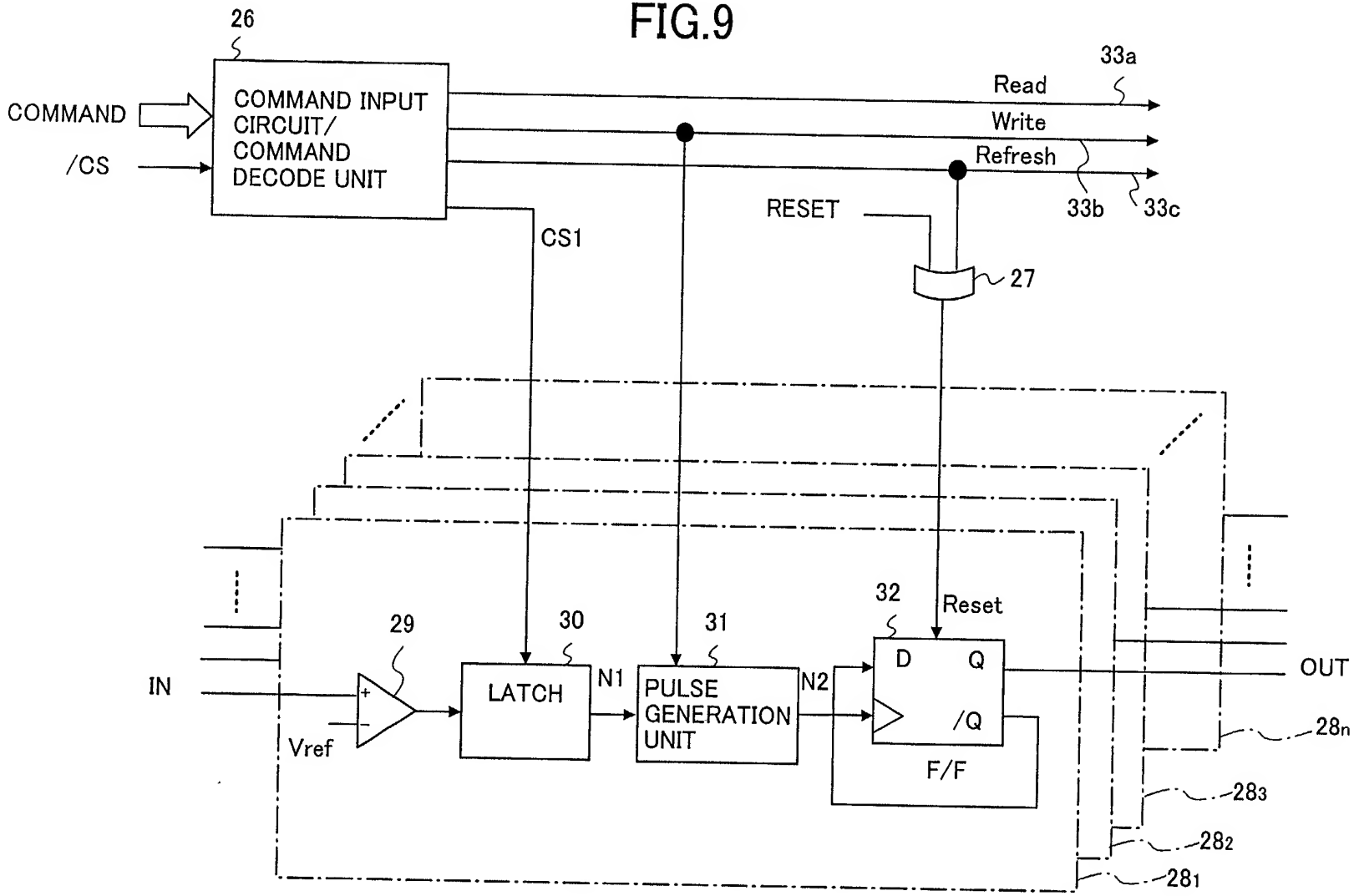

45
30
SYNCHRONOUS LATCH
N7
55b
55a
49a
49b
53a
53b
50b
Delay
48a
58
52a
Delay
54b
50a
57
48b
52b
54a
47a
51a
CLK2
/CLK2
29
+
−
Vref
IN

FIG.9


26
COMMAND
/CS
COMMAND INPUT CIRCUIT/ COMMAND DECODE UNIT
33a
Read
Write
Refresh
33b
33c
RESET
27
CS1
IN
29
Vref
30
LATCH
N1
31
PULSE GENERATION UNIT
N2
32
Reset
D
Q
/Q
F/F
OUT
28n
283
282
281

TOSHIBA

FIG. 10

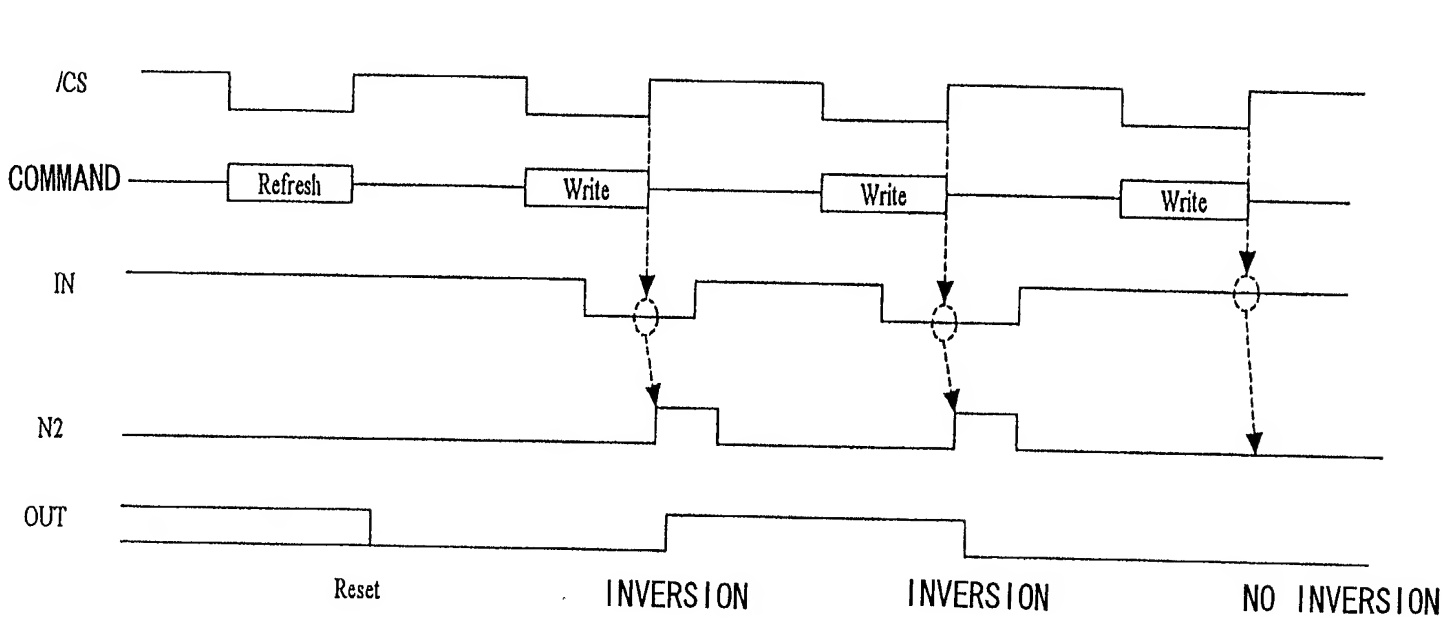


FIG.11

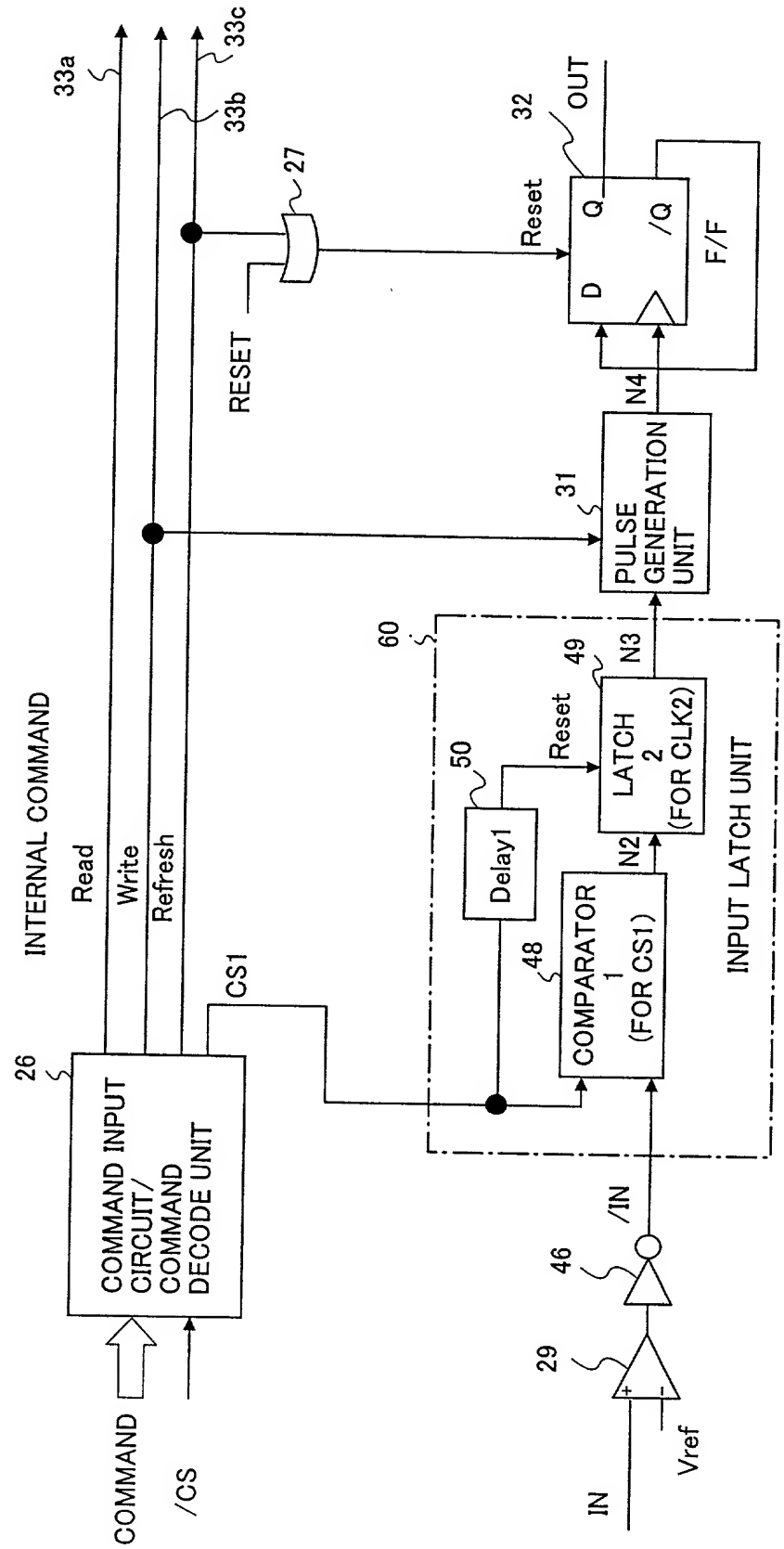

COMMAND
/CS
COMMAND INPUT CIRCUIT/ COMMAND DECODE UNIT
26
INTERNAL COMMAND
Read
Write
Refresh
CS1
33a
33b
33c
RESET
27
Reset
32
OUT
Q
/Q
D
F/F
31
PULSE GENERATION UNIT
N4
60
49
N3
LATCH 2 (FOR CLK2)
Reset
50
Delay1
48
COMPARATOR 1 (FOR CS1)
N2
INPUT LATCH UNIT
/IN
46
29
IN
Vref

FIG. 12

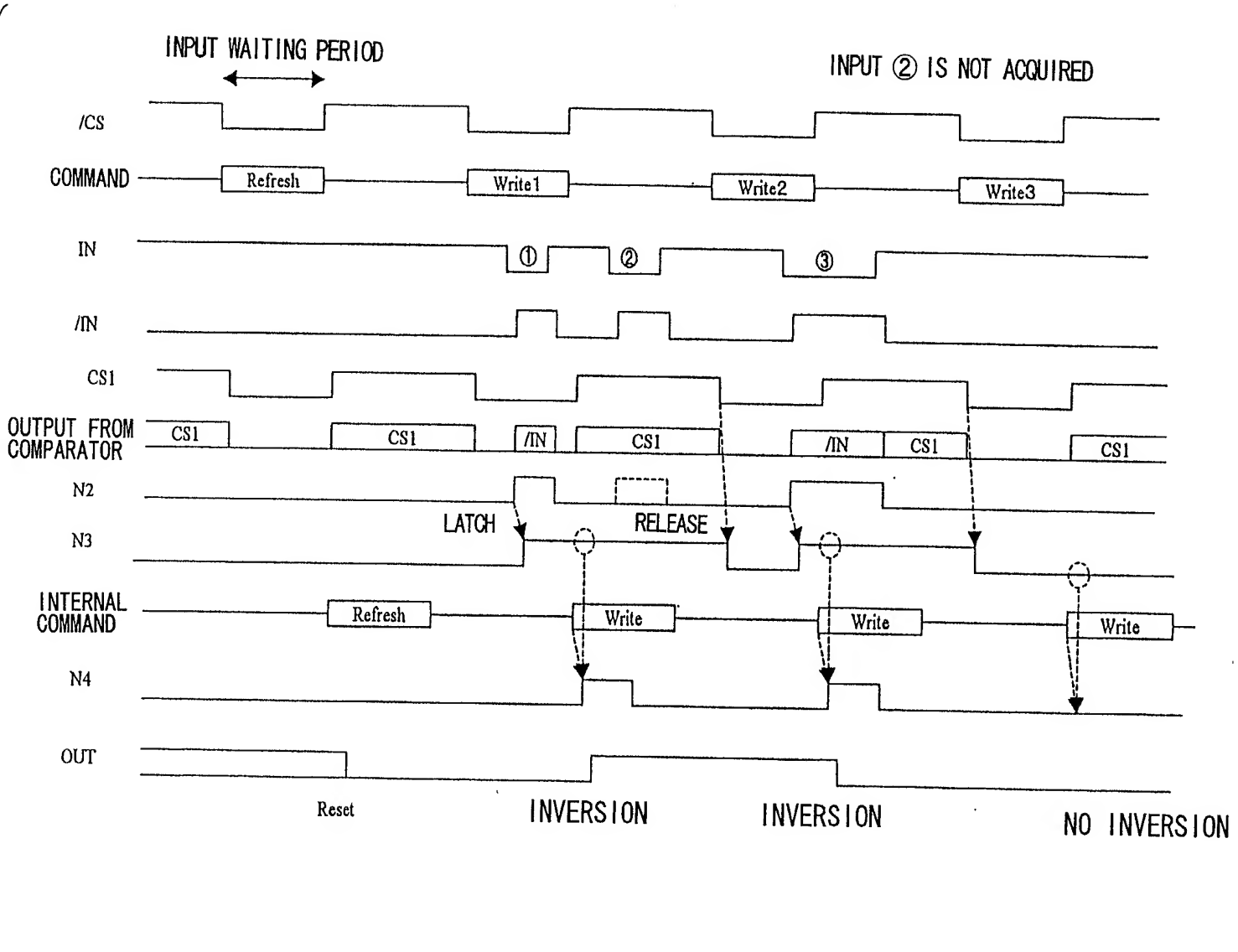

INPUT WAITING PERIOD
INPUT ② IS NOT ACQUIRED
/CS
COMMAND
Refresh
Write1
Write2
Write3
IN
①
②
③
/IN
CS1
OUTPUT FROM COMPARATOR
CS1
CS1
/IN
CS1
/IN
CS1
CS1
N2
LATCH
RELEASE
N3
INTERNAL COMMAND
Refresh
Write
Write
Write
N4
OUT
Reset
INVERSION
INVERSION
NO INVERSION

FIG.13

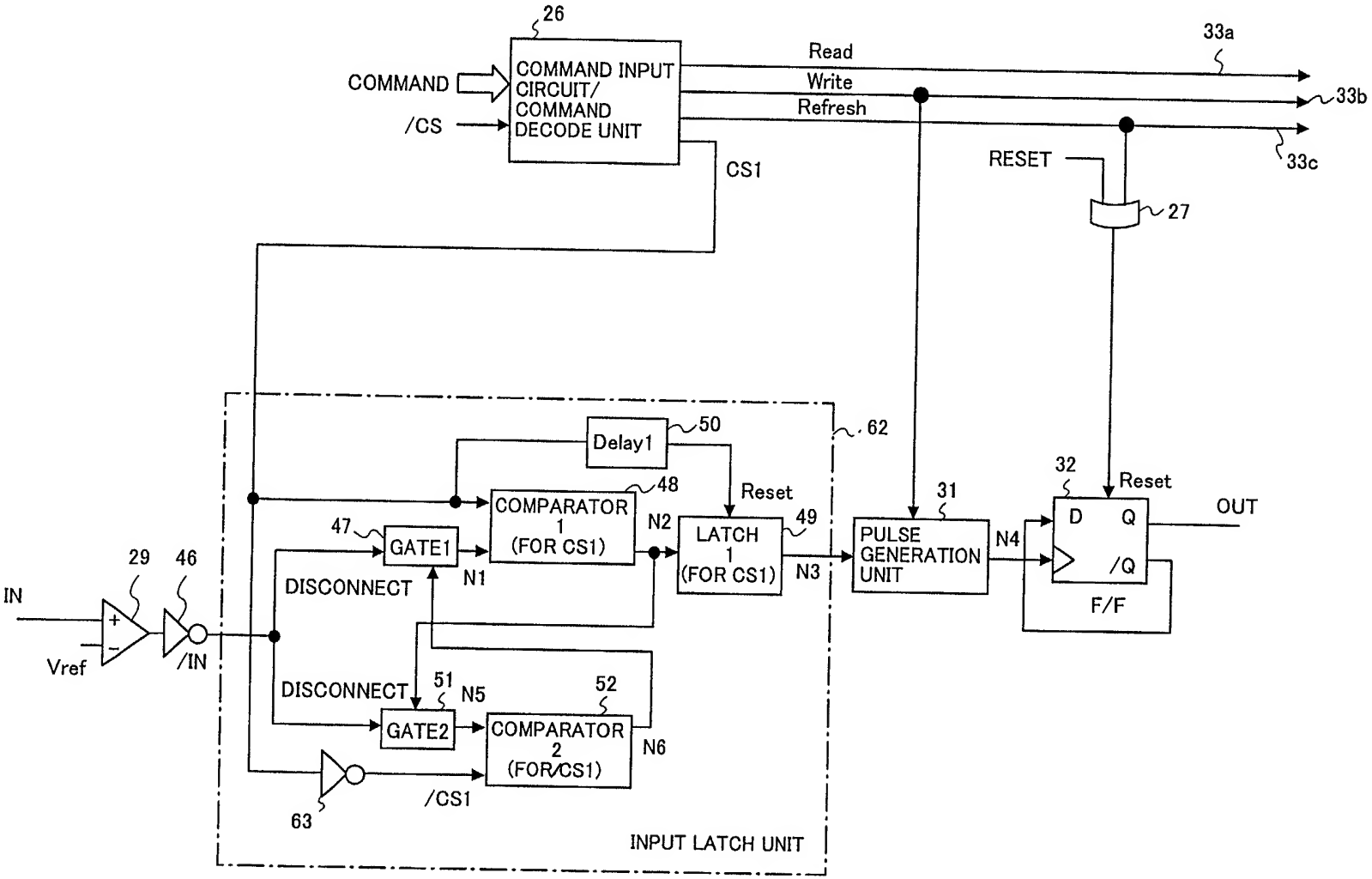
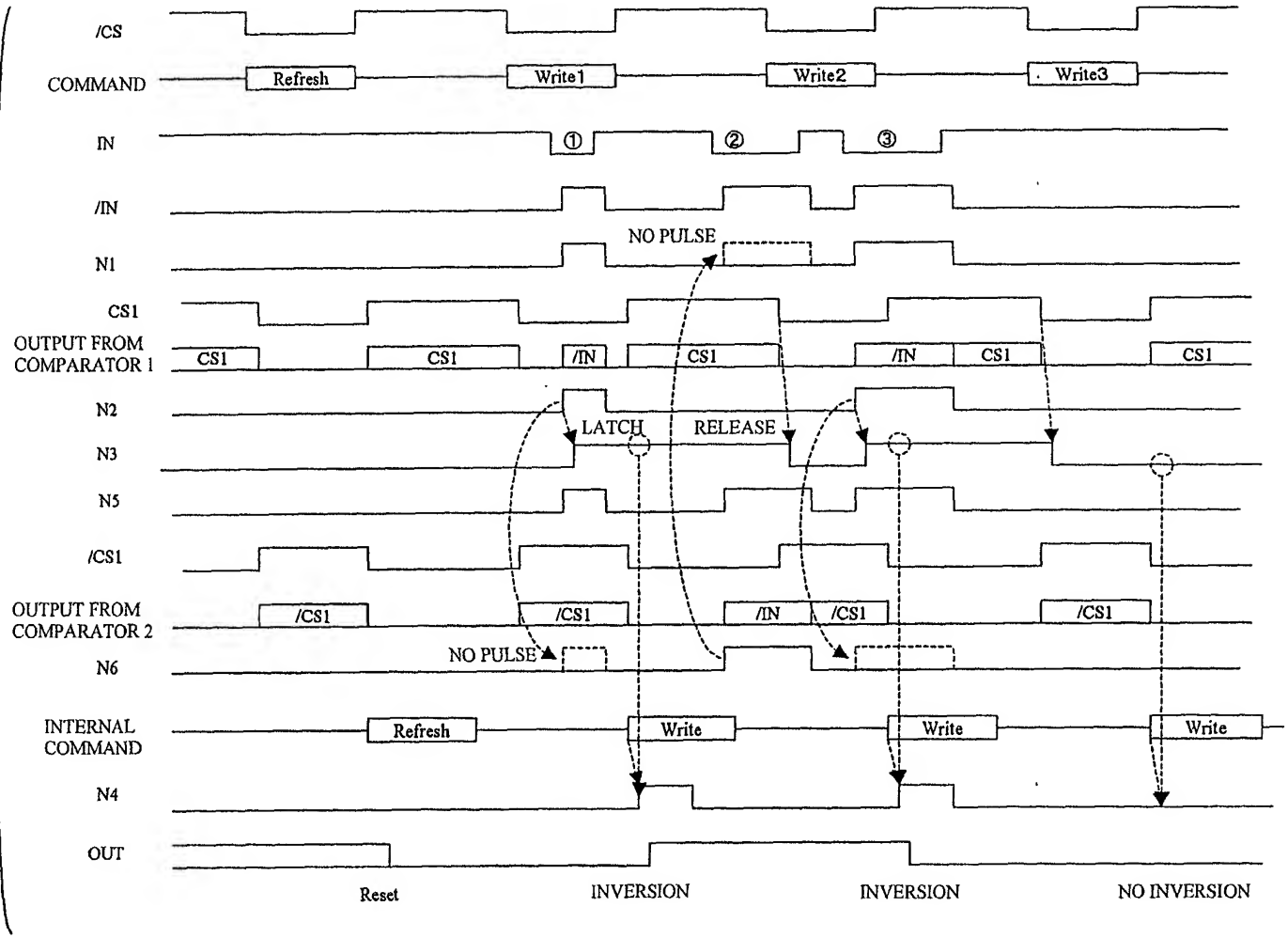

26
COMMAND
/CS
COMMAND INPUT CIRCUIT/ COMMAND DECODE UNIT
Read
Write
Refresh
33a
33b
33c
CS1
RESET
27
62
Delay1
50
Reset
48
COMPARATOR 1 (FOR CS1)
47
GATE1
N1
N2
LATCH 1 (FOR CS1)
49
N3
31
PULSE GENERATION UNIT
N4
32
Reset
D
Q
/Q
F/F
OUT
IN
29
46
Vref
/IN
DISCONNECT
DISCONNECT
51
N5
52
GATE2
COMPARATOR 2 (FOR/CS1)
N6
/CS1
63
INPUT LATCH UNIT

FIG.14


/CS
COMMAND
Refresh
Write1
Write2
Write3
IN
①
②
③
/IN
NO PULSE
N1
CS1
OUTPUT FROM COMPARATOR 1
CS1
CS1
/IN
CS1
/IN
CS1
CS1
N2
LATCH
RELEASE
N3
N5
/CS1
OUTPUT FROM COMPARATOR 2
/CS1
/CS1
/IN
/CS1
/CS1
NO PULSE
N6
INTERNAL COMMAND
Refresh
Write
Write
Write
N4
OUT
Reset
INVERSION
INVERSION
NO INVERSION

Patent Application

FIG.15

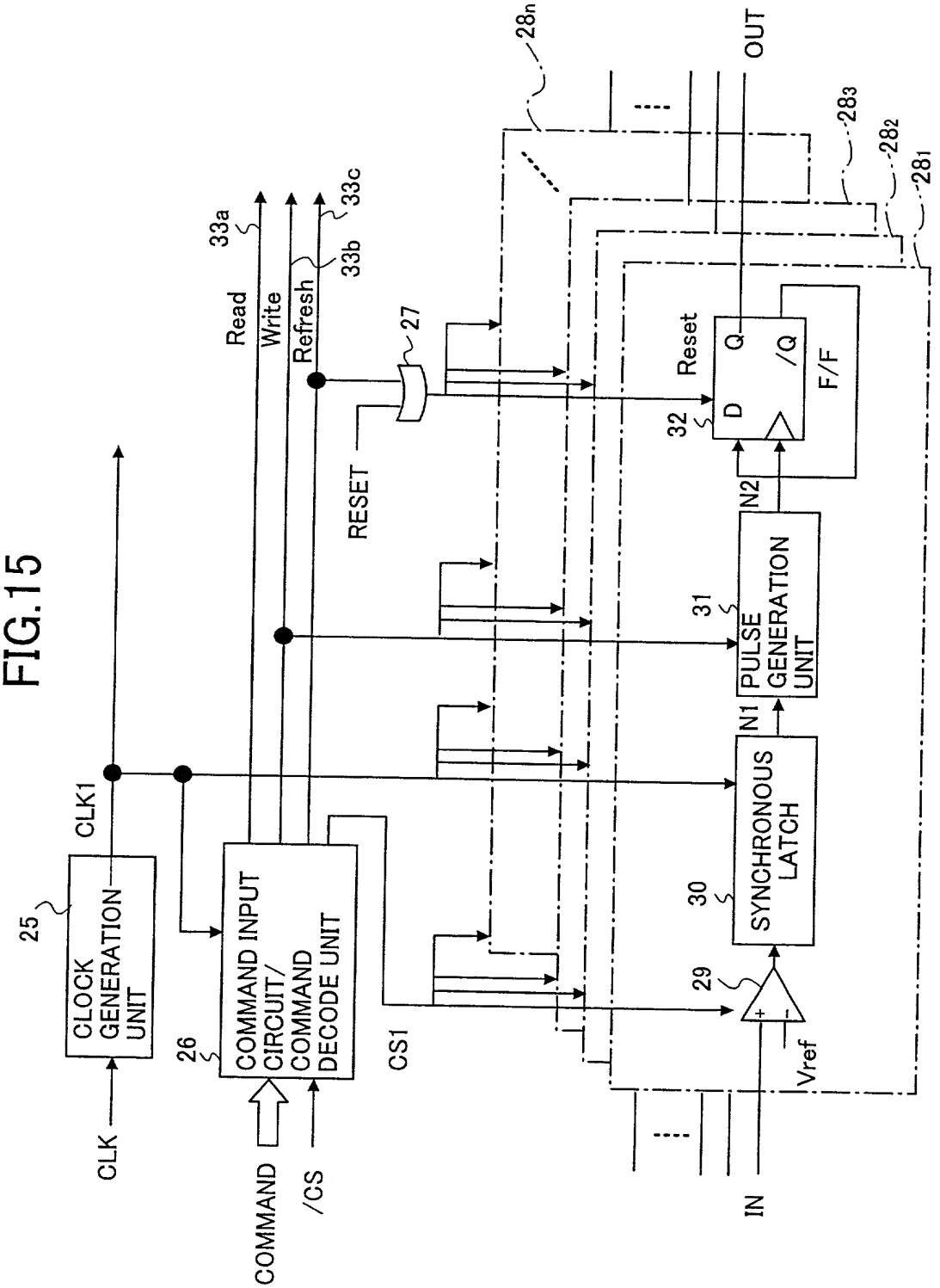


FIG. 16

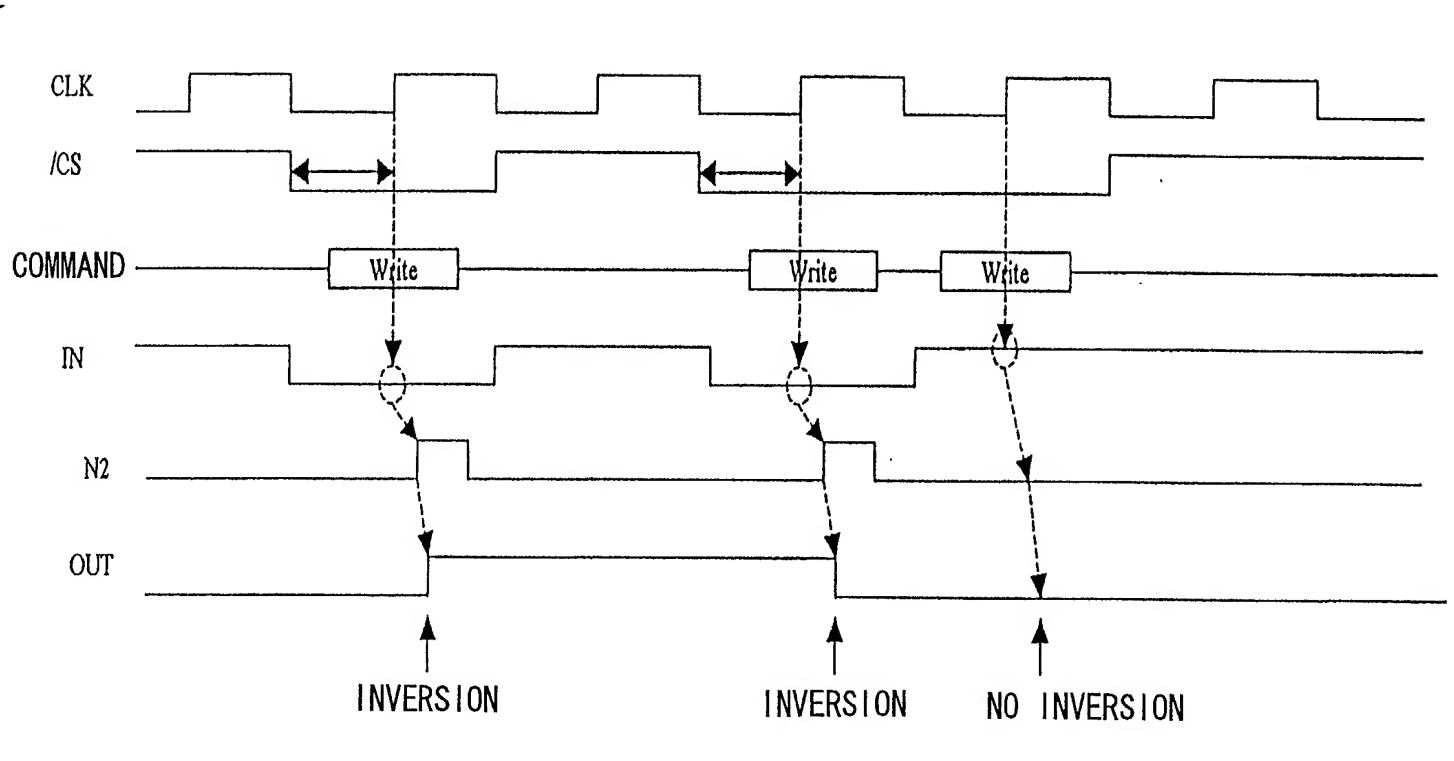

CLK
/CS
COMMAND
Write
Write
Write
IN
N2
OUT
INVERSION
INVERSION
NO INVERSION

FIG.17A

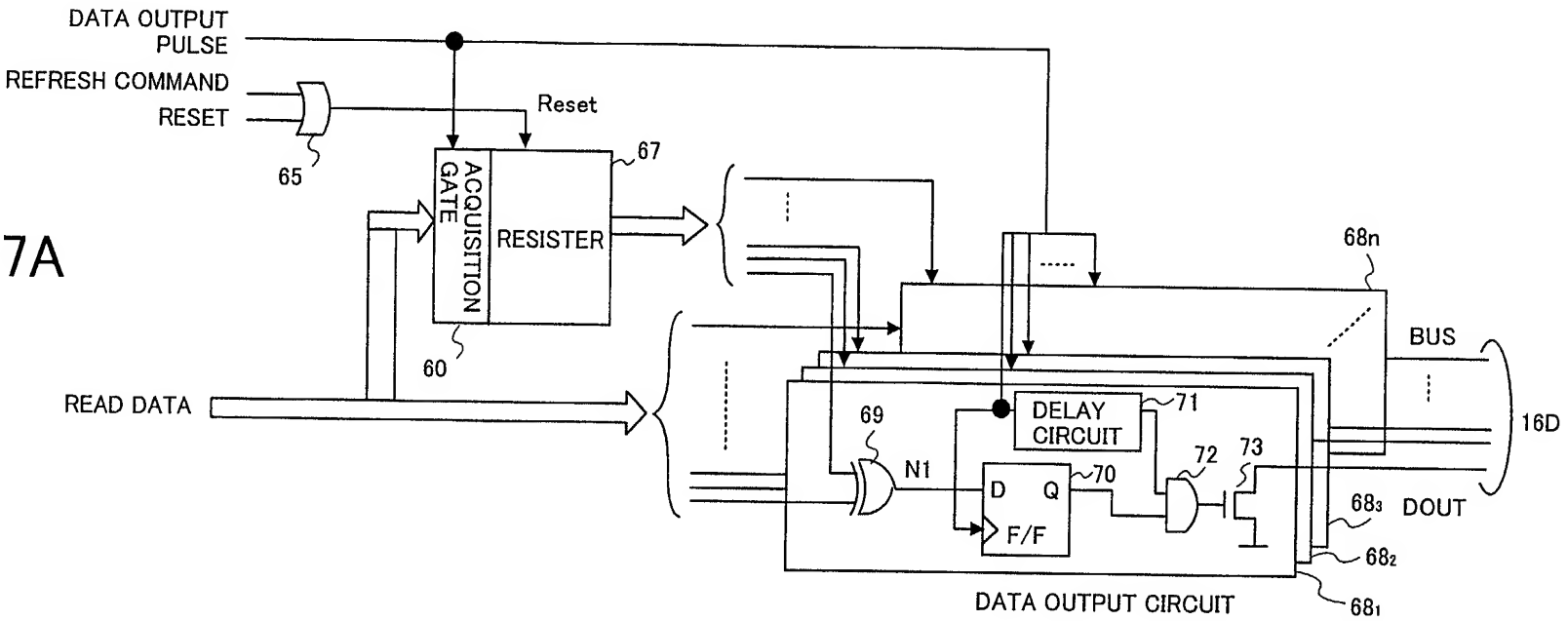


FIG.17B

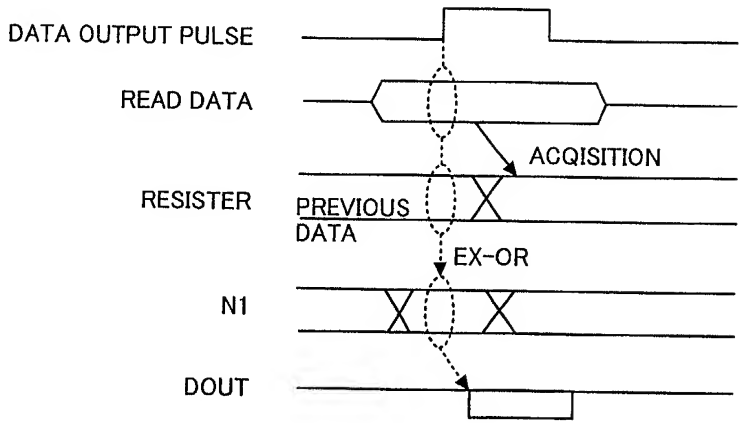


FIG.18

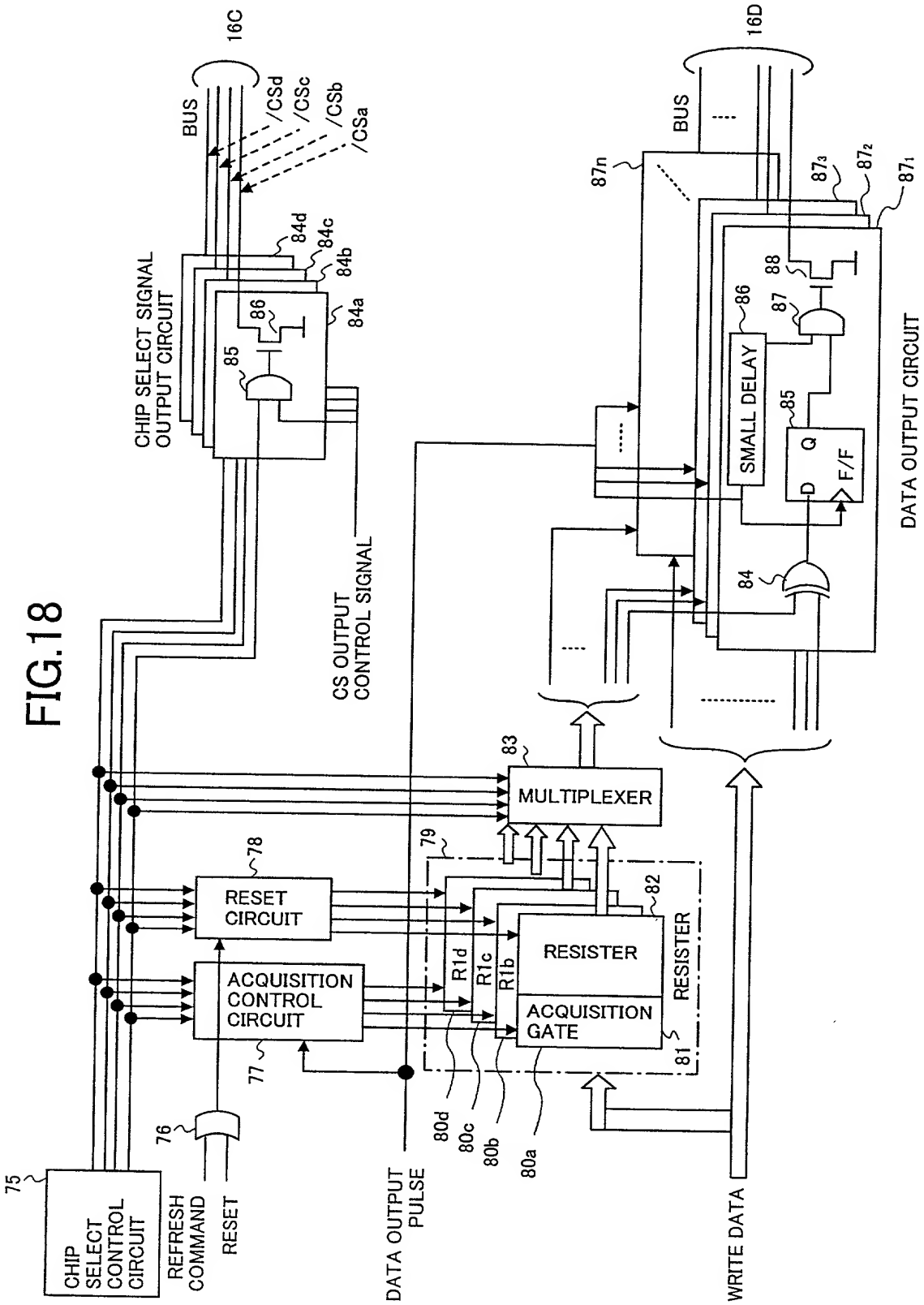

16C
BUS
/CSd
/CSc
/CSb
/CSa
84d
84c
84b
84a
86
85
CHIP SELECT SIGNAL OUTPUT CIRCUIT
CS OUTPUT CONTROL SIGNAL
16D
BUS
87n
87₃
87₂
87₁
88
86
87
SMALL DELAY
85
Q
D
F/F
DATA OUTPUT CIRCUIT
84
83
MULTIPLEXER
79
78
RESET CIRCUIT
82
RESISTER
R1d
R1c
R1b
RESISTER
ACQUISITION CONTROL CIRCUIT
ACQUISITION GATE
81
77
80d
80c
80b
80a
76
75
CHIP SELECT CONTROL CIRCUIT
REFRESH COMMAND
RESET
DATA OUTPUT PULSE
WRITE DATA

FIG.19

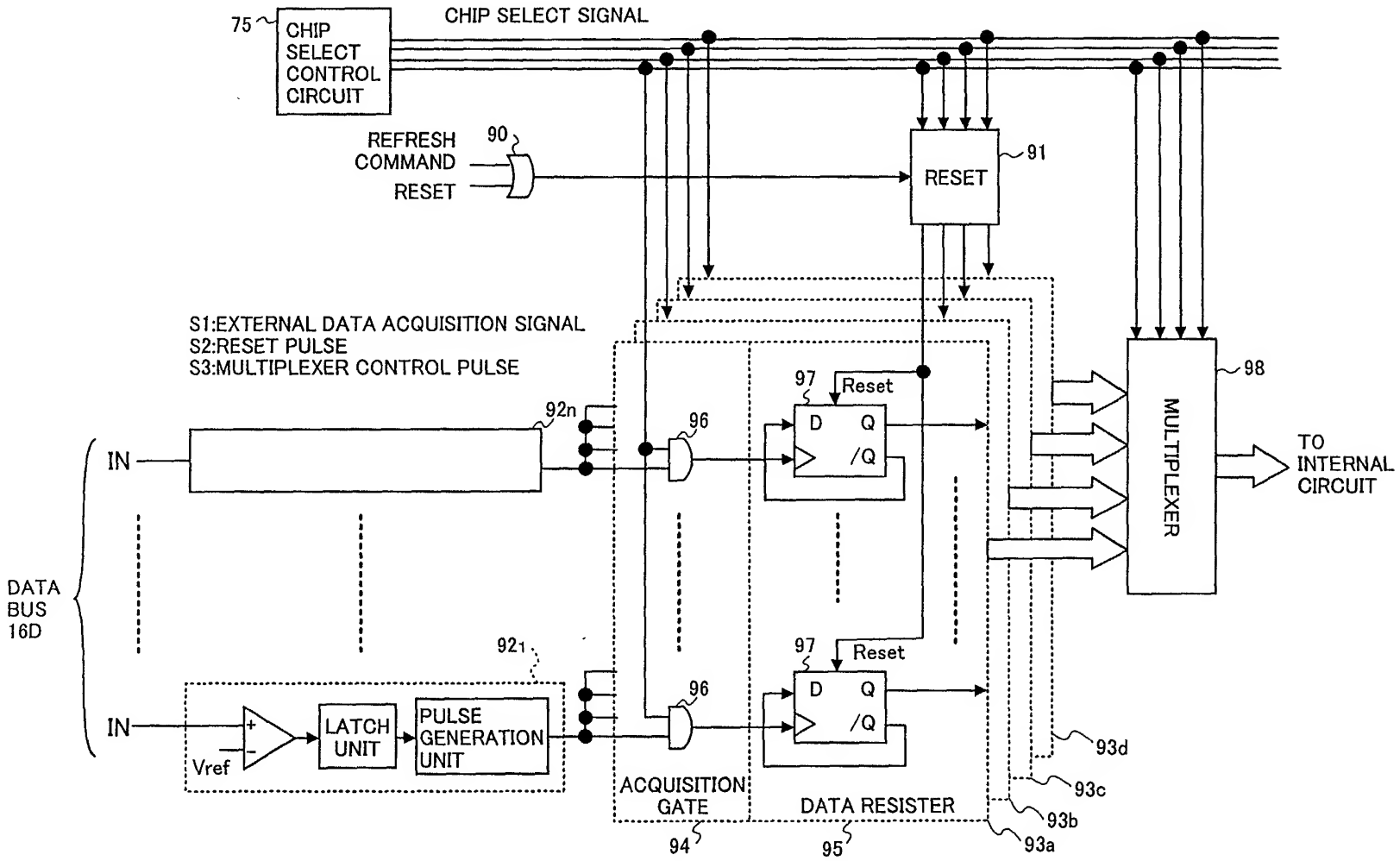

75
CHIP SELECT CONTROL CIRCUIT
CHIP SELECT SIGNAL
REFRESH COMMAND
RESET
90
91
RESET
S1:EXTERNAL DATA ACQUISITION SIGNAL
S2:RESET PULSE
S3:MULTIPLEXER CONTROL PULSE
97
Reset
D
Q
/Q
92n
96
98
MULTIPLEXER
TO INTERNAL CIRCUIT
IN
DATA BUS 16D
92₁
IN
LATCH UNIT
PULSE GENERATION UNIT
Vref
93d
93c
93b
93a
ACQUISITION GATE
94
DATA RESISTER
95

FIG.20

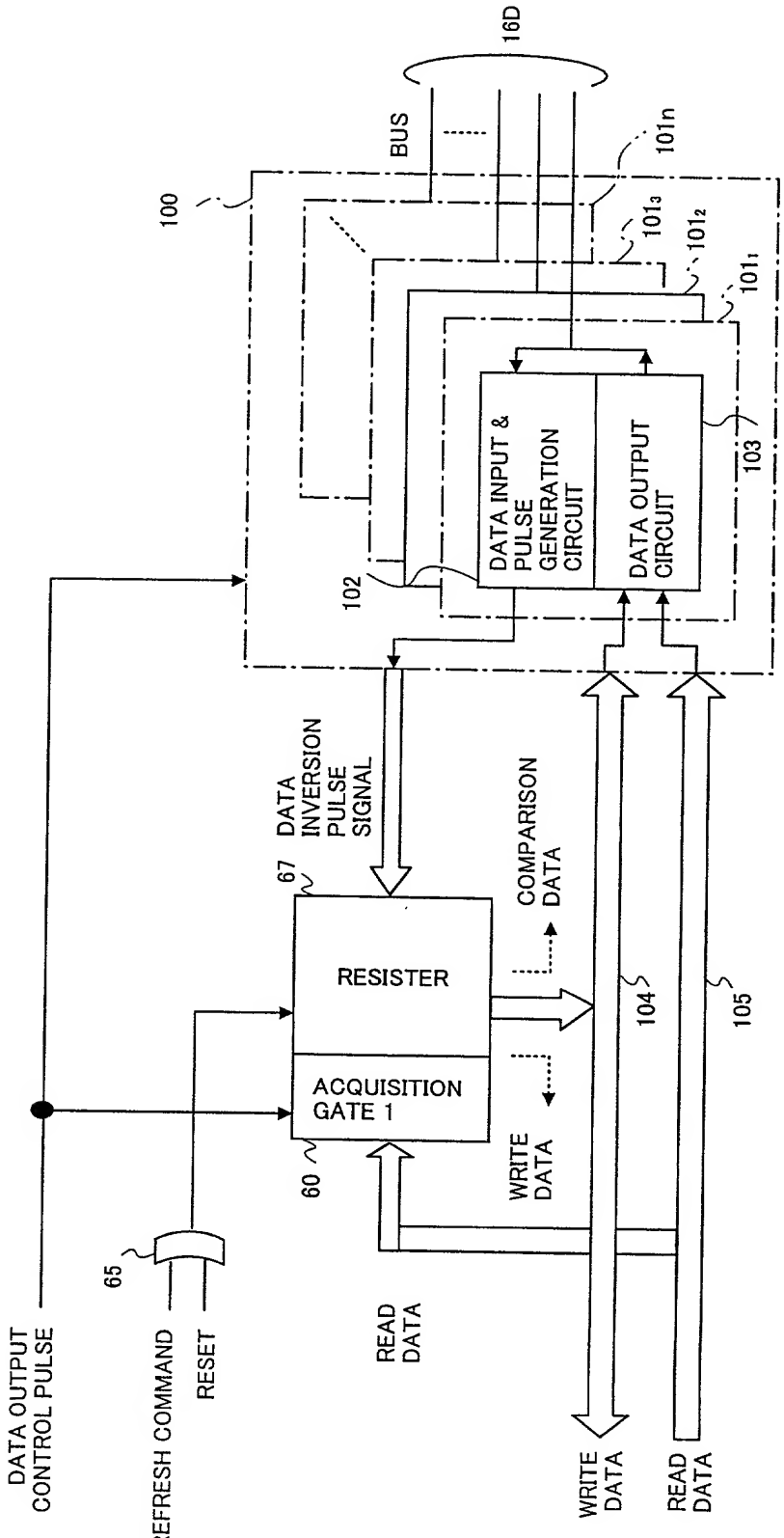
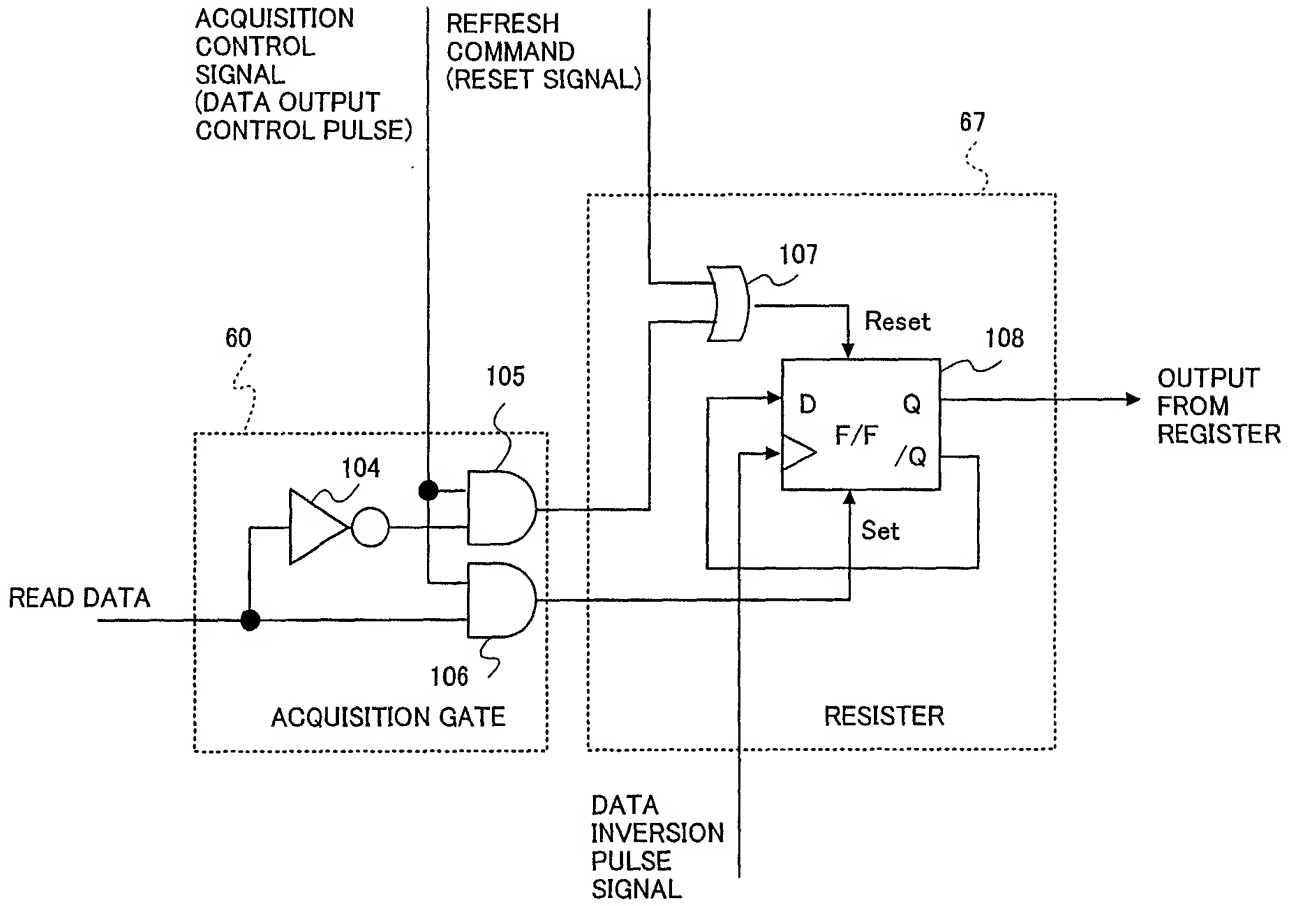

16D
BUS
100
101n
101₃
101₂
101₁
DATA INPUT & PULSE GENERATION CIRCUIT
DATA OUTPUT CIRCUIT
103
102
DATA INVERSION PULSE SIGNAL
67
COMPARISON DATA
RESISTER
ACQUISITION GATE 1
60
WRITE DATA
104
105
65
READ DATA
DATA OUTPUT CONTROL PULSE
REFRESH COMMAND
RESET
WRITE DATA
READ DATA

FIG.21


ACQUISITION CONTROL SIGNAL (DATA OUTPUT CONTROL PULSE)
REFRESH COMMAND (RESET SIGNAL)
67
107
Reset
108
60
105
D
Q
F/F
/Q
OUTPUT FROM REGISTER
104
Set
READ DATA
106
ACQUISITION GATE
RESISTER
DATA INVERSION PULSE SIGNAL

Toppan Printing

FIG.22

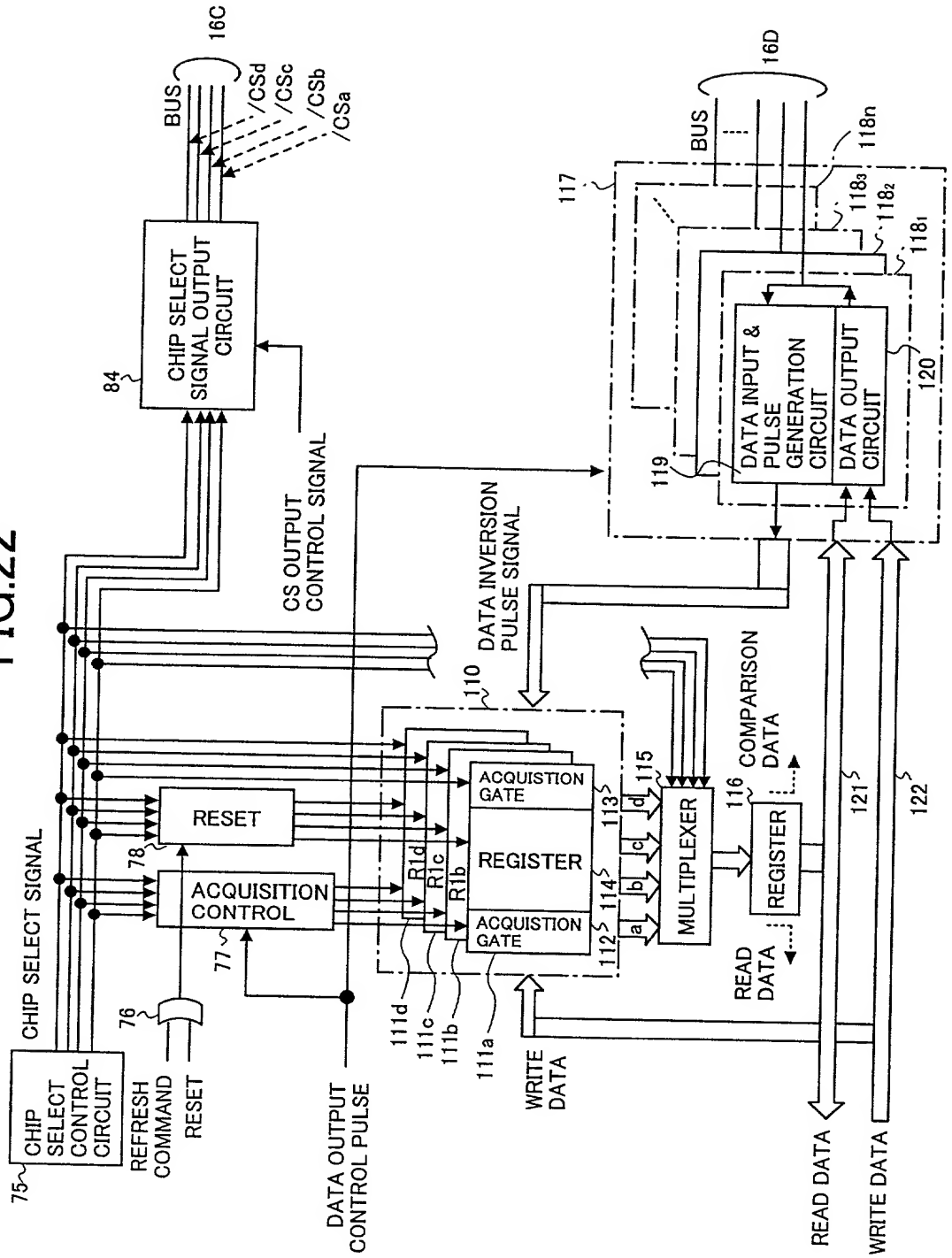


FIG.23

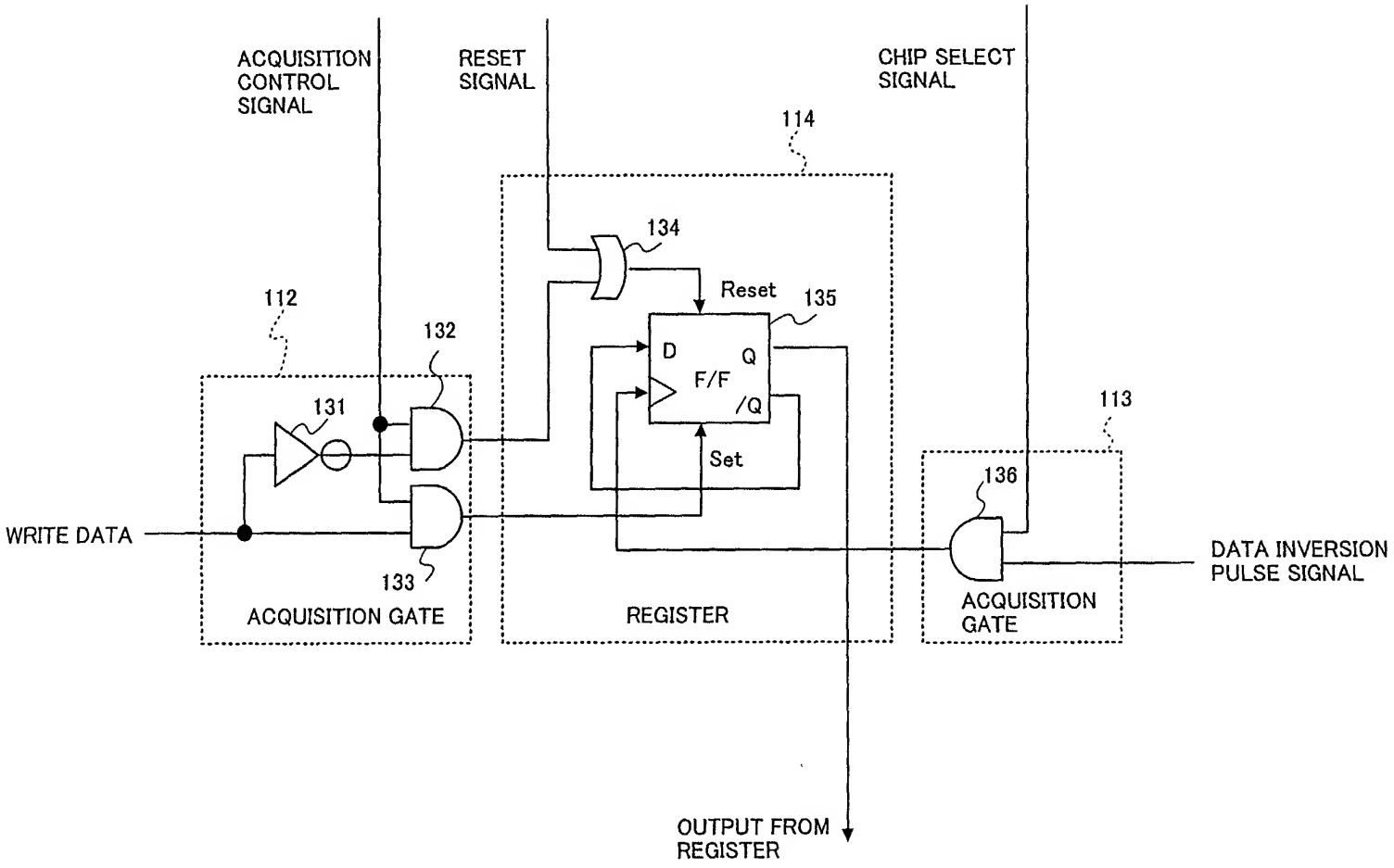

ACQUISITION CONTROL SIGNAL
RESET SIGNAL
CHIP SELECT SIGNAL
114
134
Reset
135
112
132
D
Q
F/F
/Q
131
113
Set
136
WRITE DATA
DATA INVERSION PULSE SIGNAL
133
ACQUISITION GATE
REGISTER
ACQUISITION GATE
OUTPUT FROM REGISTER

FIG.24A

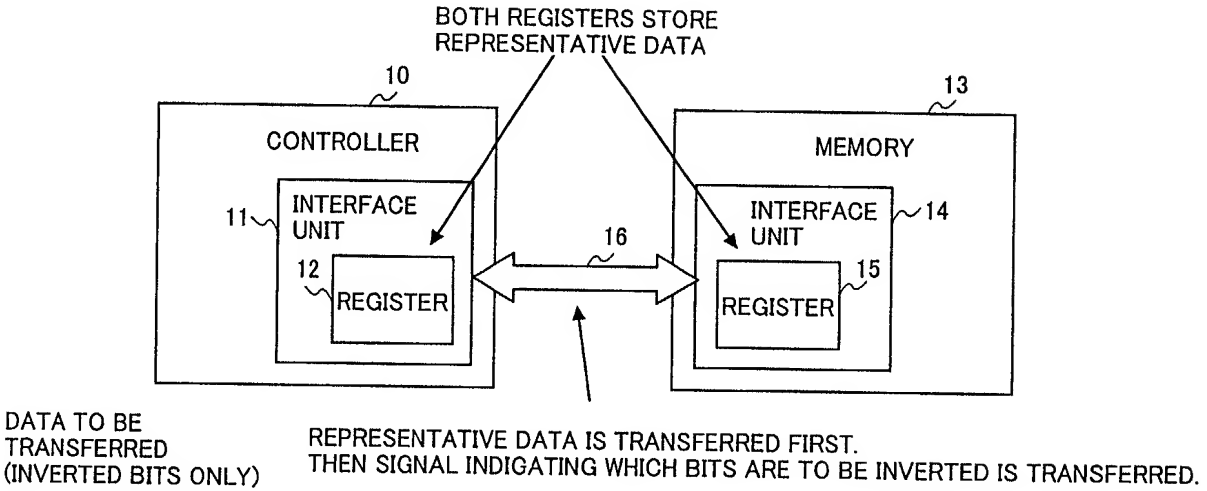


FIG.24B

CONTROLLER 10			DATA BUS 16	MEMORY 13	
COMMAND	WRITE DATA	REGISTER 12 OF CONTROLLER	DATA TRANSFERRED (INVERTED BITS ONLY)	REGISTER 15 OF MEMORY	TO MEMORY CORE
① WRITE(A)	1011	1011	1011(*1)	1011	1011
② WRITE(B)	1010	1011 EX-OR	0001(*2)	1011 EX-OR	1010
③ WRITE(B)	1000	1011 EX-OR	0011(*2)	1011 EX-OR	1000
④ WRITE(B)	0001	1011 EX-OR	1001(*2)	1011 EX-OR	0001

*1:REPRESTENATIVE DATA IS TRANSFERRED IN RESPONSE TO COMMAND WRITE(A).
*2:INVERTED DATA IS TRANSFERRED IN RESPONSE TO COMMAND WRITE(B).

FIG.25

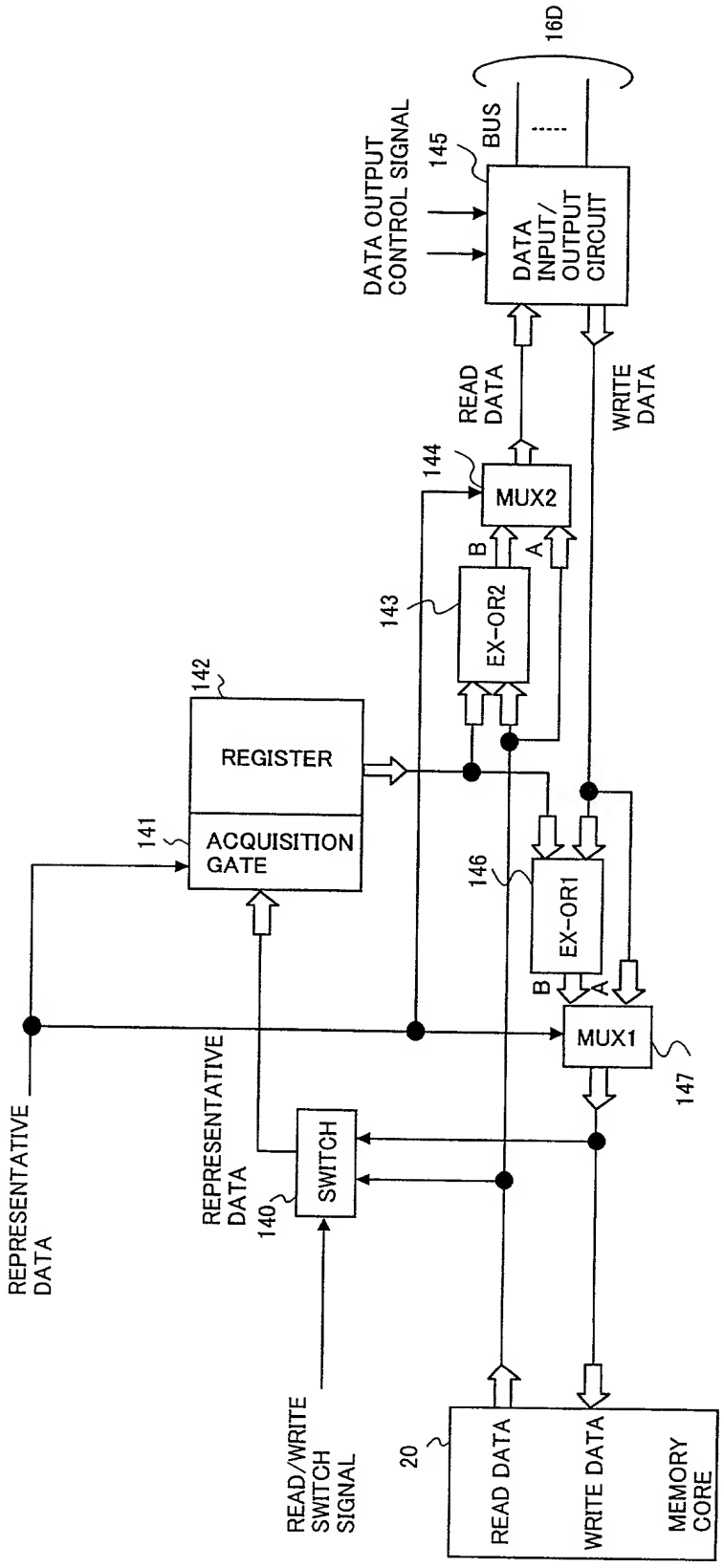

16D
BUS
145
DATA OUTPUT CONTROL SIGNAL
DATA INPUT/ OUTPUT CIRCUIT
READ DATA
WRITE DATA
144
MUX2
B
A
143
EX-OR2
142
REGISTER
141
ACQUISITION GATE
146
EX-OR1
B
A
MUX1
147
REPRESENTATIVE DATA
REPRESENTATIVE DATA
140
SWITCH
READ/WRITE SWITCH SIGNAL
20
READ DATA
WRITE DATA
MEMORY CORE

FIG.26

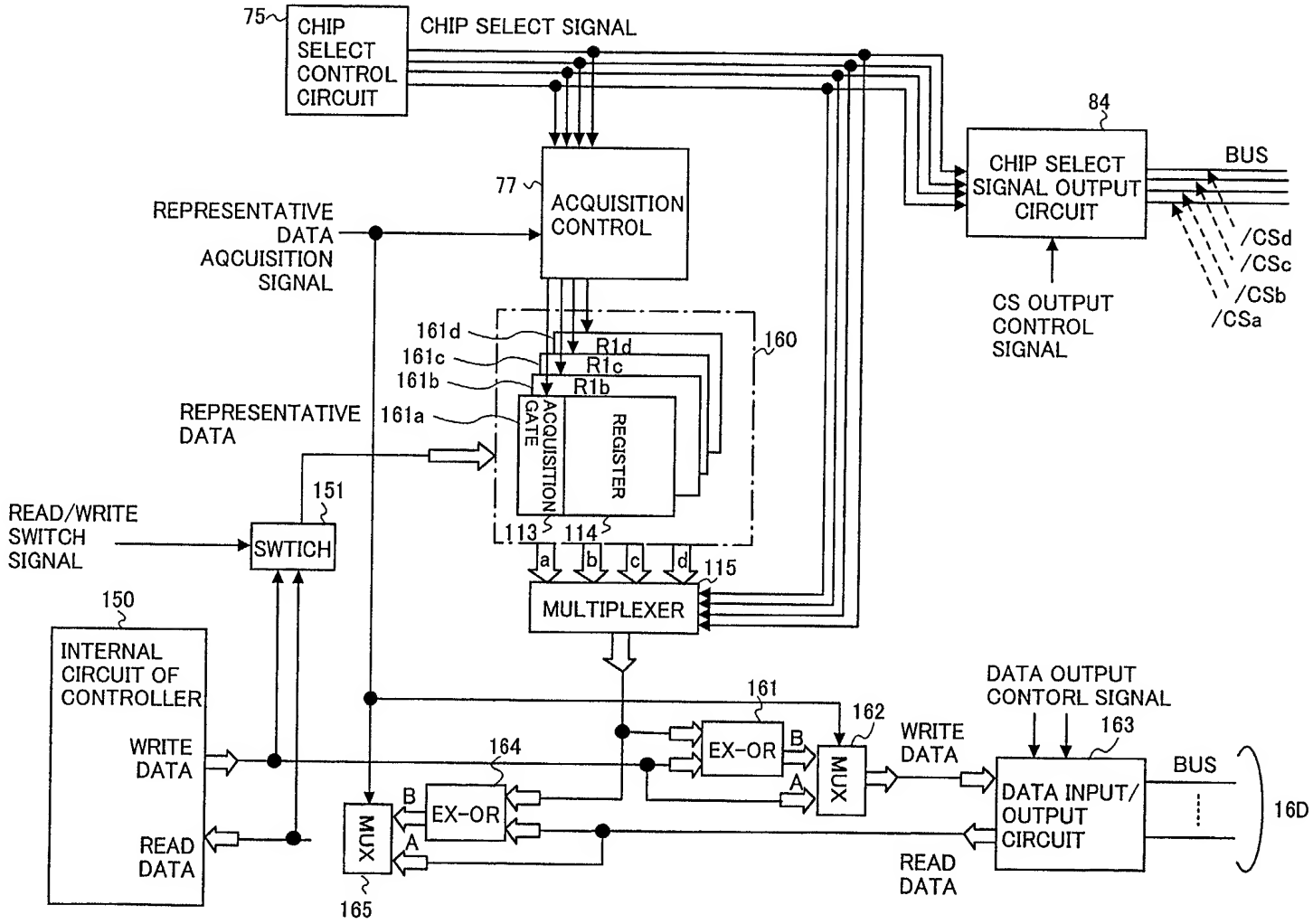
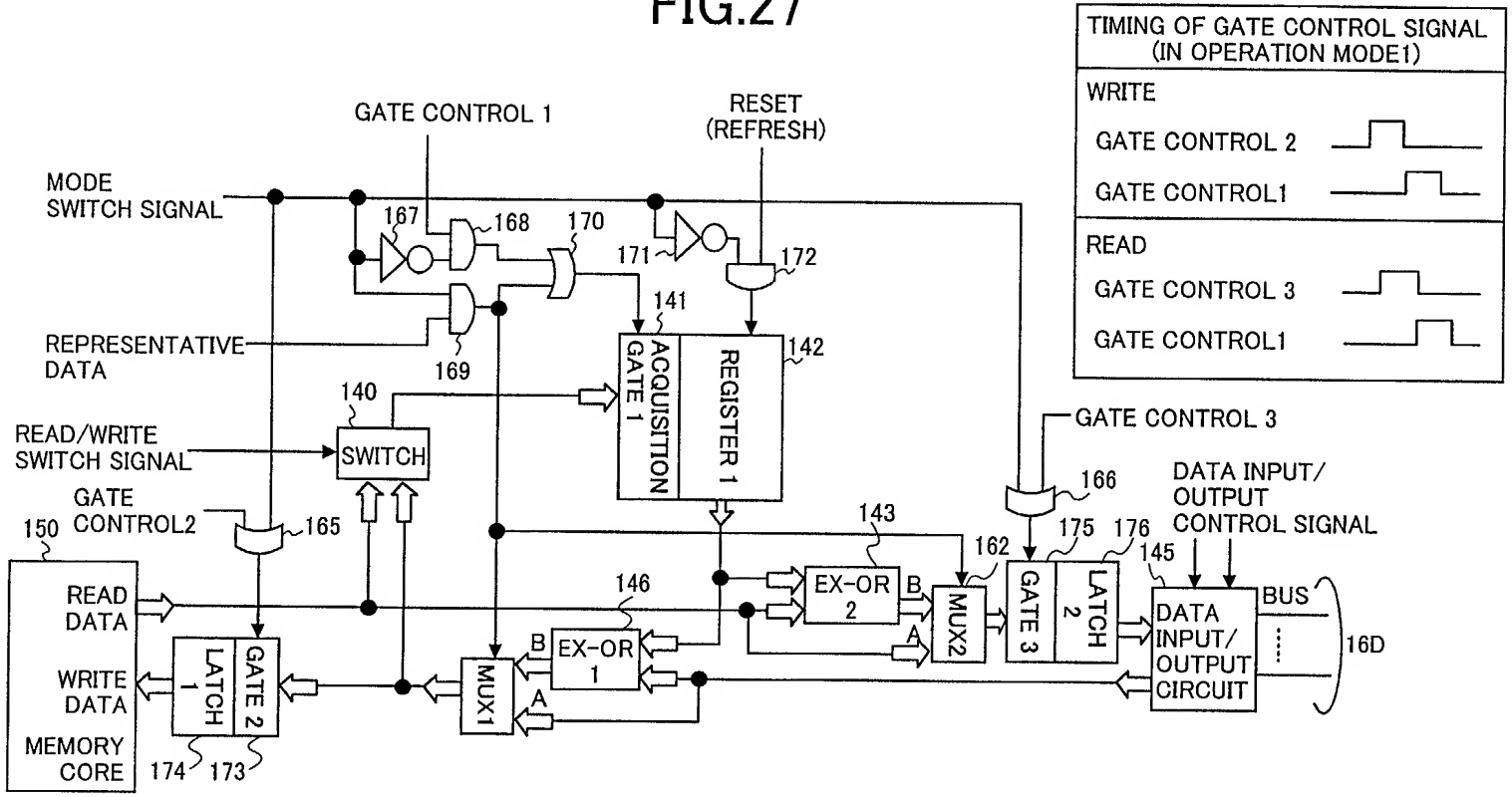

75
CHIP SELECT CONTROL CIRCUIT
CHIP SELECT SIGNAL
84
CHIP SELECT SIGNAL OUTPUT CIRCUIT
BUS
/CSd
/CSc
/CSb
/CSa
CS OUTPUT CONTROL SIGNAL
77
ACQUISITION CONTROL
REPRESENTATIVE DATA AQCUISITION SIGNAL
161d
161c
161b
161a
R1d
R1c
R1b
160
ACQUISITION GATE
REGISTER
REPRESENTATIVE DATA
151
READ/WRITE SWITCH SIGNAL
SWTICH
113
114
a
b
c
d
115
MULTIPLEXER
150
INTERNAL CIRCUIT OF CONTROLLER
WRITE DATA
READ DATA
161
162
164
EX-OR
B
A
MUX
DATA OUTPUT CONTORL SIGNAL
163
WRITE DATA
DATA INPUT/ OUTPUT CIRCUIT
BUS
16D
READ DATA
165

FIG.27



OPERATION MODE 1
(CORRESPONDING TO FIRST PRINCIPLE)

MODE SWITCH SIGNAL=LOW
ACQUISTION GATE 1: CONTROLLED BY GATE CONTROL 1 SIGNAL
MUX1,MUX2 : INPUT B IS SELECTED(FIXED)
GATE 2: CONTROLLED BY GATA CONTROL 2 SIGNAL
GATE 3: CONTROLLED BY GETA CONTROL 3 SIGNAL
REGISTER 1 IS RESET IN RESPONSE TO REFRESH

OPERATION MODE 2
(CORRESPONDING TO SECOND PRINCIPLE)

MODE SWITCH SIGNAL = HIGH
ACQUISITION GATE 1, MUX1, MUX2: CONTROLLED BY REPRESENTATIVE DATA ACQUISITION SIGNAL
GATE 2, GATE 3: OPEN (FIXED)
REGISTER 1 IS NOT RESET IN RESPONSE TO REFRESH